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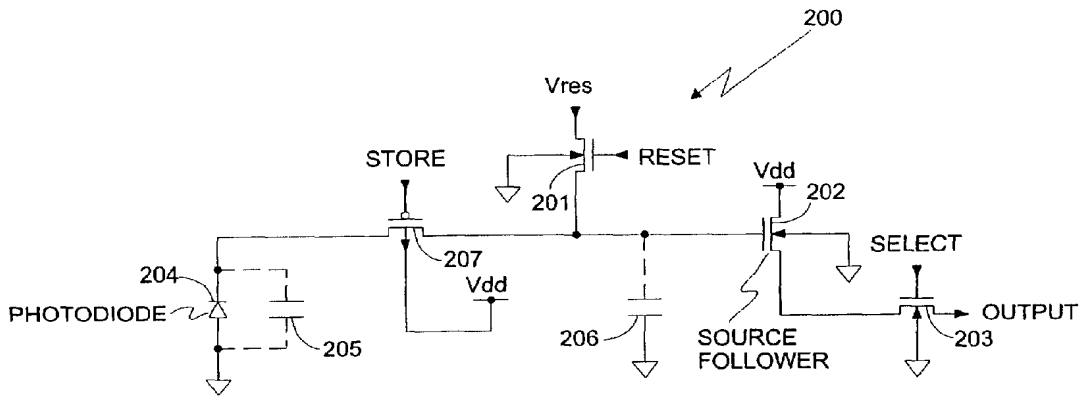
(54) Title: ACTIVE PIXEL CELL WITH CHARGE STORAGE



(57) Abstract: A CMOS four-transistor active pixel cell (APC) for use in an image sensor array is described. It includes an additional PMOS transistor with in a standard three-transistor pixel cell. The PMOS transistor acts as a typical switch to either connect or disconnect the photodiode capacitance and the gate capacitance of the three-transistor pixel cell source follower, and further reduces the photo-current discharging of the gate capacitance during the storage time. This time is dependent on the physical characteristics of the source follower transistor.

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ACTIVE PIXEL CELL WITH CHARGE STORAGE

Field of the Invention

This invention relates to the field of image processing and specifically the active pixel cell architecture that converts an optical image into an electrical signal.

Background of the Invention

CMOS image sensors are integrated circuits designed specifically to capture and process incident light. The core of the sensor is generally made up of an array of pixels or picture elements. The pixels comprise photodiodes to sense the light, and CMOS transistors that take care of the amplification and transfer of the signal sensed by the photodiode.

As light strikes the array of pixels, it is converted into photo-current, which in turn gets converted into digitized data by an Analog-to-Digital Converter (ADC). The pixel arrays are based on either active or passive pixel sensors. Passive pixel sensors do not amplify the photodiode's signal within them, whereas, active pixel sensors include amplification circuitry within the pixel.

Figure **1** illustrates a standard prior art three-transistor active pixel cell **100**. It includes a photodiode **104** and three transistors **101, 102** and **103.** The photodiode **104** converts the light impinged upon it into an electrical signal. NMOS transistor **101** has its source tied to the cathode of the photodiode **104**, its drain tied to a voltage potential V_{res} and its gate tied to a reset control signal, RESET. When the RESET signal is in a high state, transistor **101** becomes active and pre-charges the photodiode's **104** capacitance (not shown) to the voltage V_{res}. A second NMOS transistor **102** is used to separate the photodiode **104** from the external circuitry at the output, i.e. image processing hardware. The NMOS transistor **102** drain is tied to the voltage supply rail, V_{DD}, its gate is tied to the cathode of the photodiode **104** and its source tied to one drain/source terminal of transistor **103**. NMOS transistor **102** is configured as a source follower to separate the potential on the photodiode **104** from a read-out circuit (not shown) connected to the output, i.e. it is acting as a buffer. Transistor **103** is a third NMOS transistor that acts as a read access transistor. One of

its source/drain terminals is tied to the drain of transistor **102**, its other drain/source terminal tied to the pixel cell output and its gate tied to a control signal, SELECT.

The diode **104** is built by doping an n^+ region onto a p-type substrate. For the diode **104** to work as a photodiode, it is reverse biased. A photodiode**104** capacitance (not shown in the diagram) is formed due to the depletion region of the p-n junction. During the reset time of the pixel **100**, the photodiode capacitance is pre-charged to a potential close to V_{res}. Once reset is complete the integration time begins, and incoming photons create a photocurrent in the depletion region that discharges the photodiode's capacitance. This discharge establishes a voltage drop in the photodiode's capacitance, which is detected after the completion of the integration time. The higher the voltage drop in the photodiode capacitance during the integration time, the higher the picture resolution is possible.

For large pixel arrays, the issue of time lag between the read-out of the first row of pixels **100** and the subsequent row becomes a problem. This becomes an even bigger issue when trying to sense moving objects, since different images are caught by consecutive rows of the sensor array, creating linear distortion of the image.

One solution is to activate all the pixels **100** at the same time and after the integration time is complete, to freeze the state of all the pixels**100** until they have all been processed. This requires the same integration time for all active pixel cells **100**. Without the use of a mechanical shutter, this is not a possibility with the classic three-transistor APC **100**.

Therefore there is a need for an APC capable of maintaining its integrated charge for the time it takes for the array of pixels to be processed.

Summary of the Invention

The invention is directed to an active pixel cell comprising a photodiode, an element for resetting the voltage on the photodiode and a capacitance for receiving the charge from across the photodiode. The pixel further includes a switch coupled between the photodiode and the capacitance having a closed position for connecting

the photodiode to the capacitance and an open position for electrically isolating the capacitance from the photodiode. With the switch in the open position the charge on the capacitance is maintained substantially constant. An amplifier provides an output signal representing the charge on the capacitance.

In accordance with an aspect of this invention, the amplifier comprises an amplifying transistor and the capacitance comprises the input capacitance of the amplifying transistor. Further, the isolating switch and the charge resetting element both comprise transistors.

In accordance with a further aspect of this invention, the transistors are CMOS transistors that may be integrated on a common substrate. In the preferred embodiment, the amplifying transistor and the resetting transistor are NMOS transistors and the isolating transistor is a PMOS transistor.

In accordance with another aspect, the invention is directed to an active CMOS pixel cell comprising a photodiode, first transistor for resetting the photodiode and a second transistor that has an input capacitance for receiving a charge from across the photodiode and that is connected to a common node with the first transistor. A third transistor, which has an open position and a closed position, is coupled between the photodiode and the common node, whereby the charge across the photodiode is applied to the input capacitance of the second transistor when the third transistor is in the closed position and the photodiode is electrically isolated from the input capacitance when the third transistor is in the open position.

In accordance with an aspect of the invention, the charge on the input capacitance is maintained substantially constant when the third transistor is in the open position. This is achieved by having a photo-leakage current from the first transistor flowing in one direction to the common node and a photo-leakage current from the third transistor flowing in an opposite direction to the common node, therby cancelling one another out. The photo-leakage currents are preferably substantially equal.

In accordance with a specific aspect of the invention, a fourth transistor is connected to the second transistor for selectively connecting the pixel to an output bus. In the preferred embodiemtn, the first, second and fourth transistors are NMOS transistors and the third transistor is a PMOS transistor.

The invention is further directed to a CMOS image sensor comprising an array of rows and columns of active pixel cells of the type defined above that are integrated on a chip.

Other aspects and advantages of the invention, as well as the structure and operation of various embodiments of the invention, will become apparent to those ordinarily skilled in the art upon review of the following description of the invention in conjunction with the accompanying drawings.

Brief Description of the Drawings

The invention will be described with reference to the accompanying drawings, wherein:

Figure 1 illustrates a standard 3-transistor active pixel cell; and

Figure 2 illustrates a 4-transistor active pixel cell in accordance with the present invention.

Detailed Description of the Invention

The present invention provides a charge storage capability for the standard three-transistor pixel cell **100** illustrated in figure **1**. This is achieved with the aid of an additional transistor that is complementary to the reset transistor. In this case, a PMOS transistor is used to complement the NMOS reset transistor. This additional transistor acts both as a typical switch to connect the photodiode capacitance with the gate capacitance of the source-follower transistor, and a device that reduces photo-current discharging of the source-follower transistor's gate capacitance. The switch is kept on during the integration time to ensure equal potentials on source-follower gate and photodiode capacitances. The pixel cell is capable of storing charge for some storage time, which is limited because of analog nature of the storage mechanism, but long enough to read out the entire pixel array. This storage time just depends on the

physical dimensions of the gate terminal of the source follower transistor. This pixel cell is also capable of maintaining the stored charge in the presence of light thus making the need for external means of cutting out the light, such as a mechanical shutter, unnecessary.

Figure **2** represents an embodiment of the present invention. The active pixel cell **200** includes a photodiode **204** and three transistors **201, 202** and **203** found in the standard three transistor APC. Photodiode **204** capacitance **205** and the gate capacitance **206** of transistor **202** are not discrete components but are the capacitances due to the depletion region of the p-n junction of photodiode **204** and the input capacitance of transistor **202** respectively. In accordance with the present invention, a transistor **207** complementary to the reset transistor **201** i.e. PMOS transistor, is introduced as the fourth transistor to modify the standard three-transistor active pixel cell **100** of figure **1**. In addition, the reset transistor **201**, the complementary transistor **207** and gate capacitance **206** all share a common node.

A transistor complementary to the reset transistor **203** is used as the switch **207**, instead of a matching transistor in order to obtain a circuit where the photo-currents that are generated in the transistor drain/source-body junctions and which flow into the common node, compensate each other.

If an NMOS transistor is used as the switch **207**, its first p-n junction is connected in parallel with the main photodiode **204** junction and the second p-n junction is connected in parallel with the source-follower transistor **202** gate capacitance **206**. This second p-n junction's photo-leakage current discharges the source-follower's gate capacitance **206** when the switch **207** is off, therefore, defeating the purpose of introducing a charge storage element.

The PMOS transistor **207** is serially connected between the cathode of the photodiode **204** and the gate of the source-follower transistor **202**. The gate of transistor **207** is connected to control signal STORE. The NMOS reset transistor **201** is connected at the common node on the line between the PMOS transistor **207** and the source-follower transistor **202**. The drain of transistor **202** is connected to the

power supply V_{DD} and its source is connected to a drain/source terminal of selection transistor **203**.

The functionality of the new 4T-pixel cell is as follows:

- During reset, both the PMOS transistor **207** and the NMOS reset transistor **201** are switched on, so a path from the reset voltage, V_{res} to the cathode of the photodiode **204** is established.

- The photodiode capacitance **205** and the source-follower's gate capacitance **206** are pre-charged to the same potential. These capacitances are not physically part of the architecture, but rather formed due to the source follower transistor's **202** input capacitance and a capacitance of the depletion region in the p-n junction of the photodiode **204**. The source follower transistor **202** is constructed in such a manner that its gate region is insensitive to the light.

- Next, the reset transistor **201** switches off and the integration time begins. The PMOS transistor **207** is still in activation and consequently, the voltage on both the photodiode and source-follower gate capacitances **205**, **206** are very close during the entire integration time. After the integration time is complete, the PMOS transistor **207** switches off. As a result, the link between both capacitances disconnects, yet the voltage on both capacitances remains the same. At this point, photo-leakage currents are responsible for the changes in voltage on the gate capacitance **206**. The photo-leakage current from the PMOS transistor's **207** p^+-body junction is charging the gate capacitance **206** and the current of the n^+-body junction of the NMOS reset transistor **201** flows in the opposite direction and discharges the gate capacitance **206**. However, when the dimensions for both p^+ and n^+ are selected adequately, in terms of their doping profiles and transistor sizes, both photo-leakage currents compensate each other, and they do not affect the potential on the gate capacitance **206**. Therefore, the gate capacitance **206** of the source-follower transistor **202** stores, for a particular time, the proper value of the pixel **200** voltage.

- The storage time can be obtained by selecting the appropriate dimensions of the gate of the source-follower transistor **202**. Once the voltage stored on the gate capacitance **206** exceeds that of the threshold voltage of source-follower **202**, this transistor will turn on and generate a current proportional to the gate capacitance **206**. When the pixel cell **200** selection signal, SELECT is in a high state, the selection transistor **203** becomes active and passes the information originally stored on both the photodiode capacitance **205** and the source follower's **202** gate capacitance **206** to the output, which is the main data bus.

While the invention has been described according to what is presently considered to be the most practical and preferred embodiments, it must be understood that the invention is not limited to the disclosed embodiments. Those ordinarily skilled in the art will understand that various modifications and equivalent structures and functions may be made without departing from the spirit and scope of the invention as defined in the claims. Therefore, the invention as defined in the claims must be accorded the broadest possible interpretation so as to encompass all such modifications and equivalent structures and functions.

What is claimed is:

1. An active pixel cell comprising:
   - photodiode means;
   - means for resetting the photodiode means;
   - capacitance means for receiving a charge from across the photodiode means;
   - switch means coupled between the photodiode means and the capacitance means having closed position for connecting the photodiode means to the capacitance means and an open position for electrically isolating the capacitance means from the photodiode means;
   - means for maintaining the charge on the capacitance means substantially constant with the switch means in the open position; and
   - means for providing a signal representing the charge on the capacitance means.

2. An active pixel cell as claimed in claim 1 wherein the signal providing means comprises an amplifying transistor.

3. An active pixel cell as claimed in claim 2 wherein the capacitance means comprises the input capacitance of the amplifying transistor.

4. An active pixel cell as claimed in claim 3 wherein the isolating switch means comprises a transistor.

5. An active pixel cell as claimed in claim 4 wherein the resetting means comprises a switch for applying a predetermined voltage to the photodiode means.

6. An active pixel cell as claimed in claim 5 wherein resetting switch comprises a transistor.

7. An active pixel cell as claimed in claim 6 wherein the amplifying transistor, the isolating transistor and the resetting transistor are CMOS transistors.

8. An active pixel cell as claimed in claim 6 wherein the amplifying transistor and the resetting transistor are NMOS transistors and the isolating transistor is a PMOS transistor.

9. An active pixel cell as claimed in claim 6 wherein the amplifying transistor, the isolating transistor, the resetting transistor and the photodiode means are CMOS transistors on a common substrate.

10. An active CMOS pixel cell comprising:
- a photodiode;
- first transistor means for resetting the photodiode;
- second transistor means having an input capacitance for receiving a charge from across the photodiode and connected to a common node with the first transistor means; and
- third transistor means having an open position and a closed position coupled between the photodiode and the common node, whereby the charge across the photodiode is applied to the input capacitance of the second transistor means when the third transistor means is in the closed position and the photodiode is electrically isolated from the input capacitance when the third transistor means is in the open position.

11. An active CMOS pixel cell as claimed in claim 10 further comprising means for maintaining the charge on the input capacitance substantially constant when the third transistor means in the open position.

12. An active CMOS pixel cell as claimed in claim 11 wherein the charge maintaining means comprises a photo-leakage current from the first transistor means flowing in one direction to the common node and a photo-leakage current from the third transistor means flowing in an opposite direction to the common node.

13. An active CMOS pixel cell as claimed in claim 12 wherein the photo-leakage currents are substantially equal.

14. An active CMOS pixel cell as claimed in claim 12 wherein the first transistor means is an NMOS transistor and the third transistor means is a PMOS transistor.

15. An active CMOS pixel cell as claimed in claim 12 which further includes a fourth transistor means connected to the second transistor means for selectively connecting the pixel to an output bus.

16. An active CMOS pixel cell as claimed in claim 15 wherein the first, second and fourth transistor means are NMOS transistors and the third transistor means is a PMOS transistor.

17. A CMOS image sensor comprising an array of rows and columns of active pixel cells as claimed in claim 1 integrated on a chip.

18. A CMOS image sensor comprising an array of rows and columns of active pixel cells as claimed in claim 10 integrated on a chip.

19. A CMOS image sensor comprising an array of rows and columns of active pixel cells as claimed in claim 14 integrated on a chip.

20. A CMOS image sensor comprising an array of rows and columns of active pixel cells as claimed in claim 16 integrated on a chip.

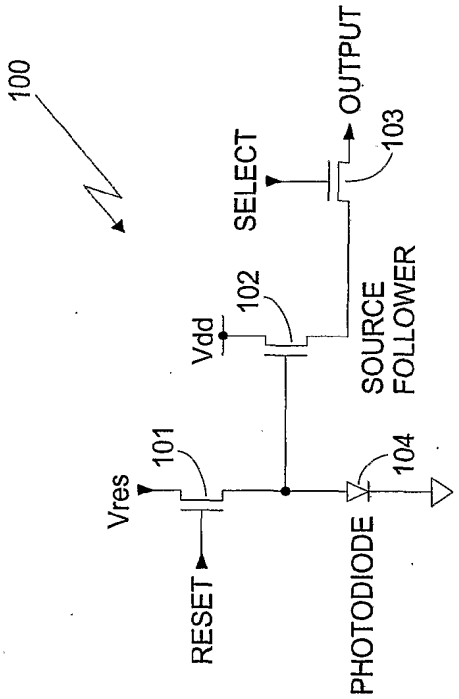

FIGURE 1 (Prior Art)

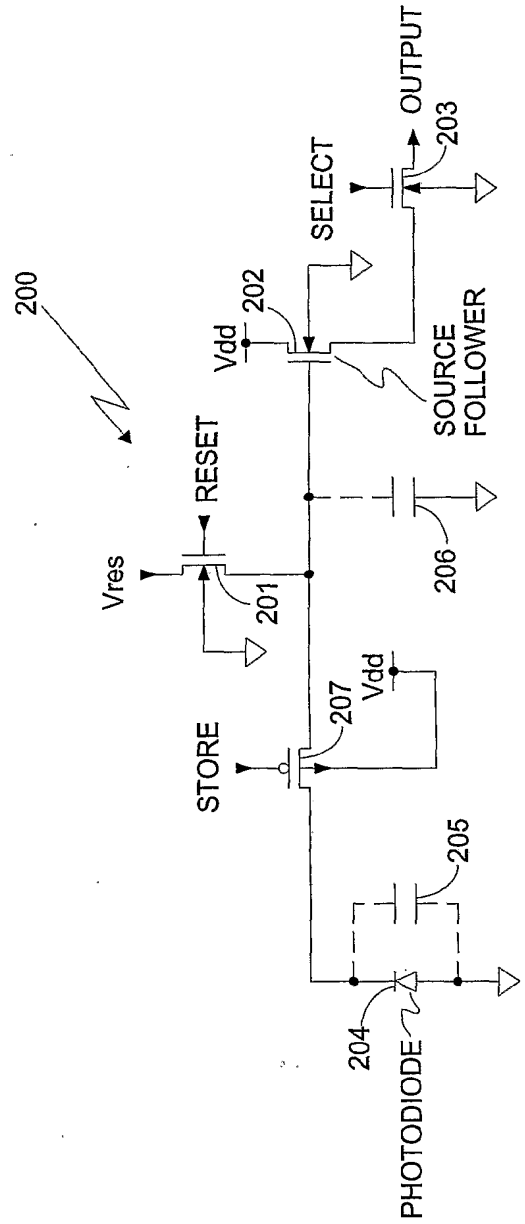
200
OUTPUT
203
SELECT
202
Vdd
SOURCE
FOLLOWER
RESET
Vres
201
206
Vdd
207
STORE
205
204
PHOTODIODE

FIGURE 2